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10/028,858	12/19/2001	Shivnandan D. Kaushik	42390P13163	4672

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EXAMINER	
ZAMAN, FAISAL M	

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10/028,858	12/19/01	Kaushik	42390P13163

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Zaman, Faisal M.	
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Commissioner for Patents

Attached is a version of the Examiner's Answer with corrected Heading 2 and Heading 11, per requirement of an Appeal Center Return. No new matter has been added or deleted from any other sections of the Examiner's Answer.

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/028,858
Filing Date: December 19, 2001
Appellant(s): KAUSHIK ET AL.

Paul A. Mendonsa (Reg. No. 42,879)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed October 6, 2006 appealing from the Office action mailed March 28, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

Appellants have indicated that in the instant application (Application Serial Number 10/028,858), Appellants had filed an Appeal Brief on July 6, 2005 in response to the Office Action dated February 7, 2005. However, since the claims on appeal have changed since then, that Appeal Brief is no longer related to the current Appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

Claims 1-10 and 16-38 are pending. Claims 16-27 and 31-34 have been allowed. Claims 1-5, 7-10, 28, 29, 35, and 37 have been rejected. Claims 6, 30, 36, and 38 have been objected to and would be allowable if rewritten in independent form to include each and every limitation of the base claim and any intervening claim.

Claims 11-15 have been canceled (Claims 1-15 were indicated as cancelled in the Appeal Brief).

Claims 1-5, 7-10, 28-29, 35, and 37 are being appealed.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,587,909	Olarig et al.	7-2003
6,282,596	Bealkowski et al.	8-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Olarig et al. ("Olarig") (U.S. Patent No. 6,587,909).

As for claim 8, Olarig teaches a method of adding memory to a running computing device (see figure 1, computer system 10, memory modules 14 and column 6 lines 50-57, wherein additional memory modules are added by hot-plugging to the computer system 10), comprising:

Identifying memory of a hot plug module in response to the hot plug module being physically coupled to the running computing device (see column 5 lines 1-23, wherein the System Control Interrupt (SCI) generates interrupt to the ACPI driver for "hot add" memory event. The ACPI driver responds to the "hot add" memory event by performing the 5 tasks, wherein the first task is to determine if memory has been added or removed and if the has been added, determine whether if it is a "hot addition" or a "hot replacement". This task is equivalent to what is claimed by identifying a memory module, which is being added or removed from the computer system 10. Furthermore, tasks 2-5 performing the memory configuration for the "hot add" memory event).

Adding the identifying memory to the hot plug module to a memory pool of the running computing device to increase the memory pool from which memory is allocated to threads (Column 5, lines 17-21, and column 3 lines 15-20, wherein the memory modules are added to the computer system as claimed), and

Enabling a communication interface on the hot plug module to establish a communication link with the running computing device (Column 6, lines 50-57, and

Column 5, lines 1-23, wherein the 5 tasks performing the configuration for establishing communication between the newly added memory module and the computer system 10).

As for claims 1, 7, and 9, Olarig teaches a method of adding one or more caching agents to a running computing device (see figure 1, memory modules 14, computer system 10), comprising:

Identifying the one or more caching agents provided by a hot plug module in response to the hot plug module being physically coupled to the running computing device (see column 5 lines 1-23, wherein the System Control Interrupt (SCI) generates interrupt to the ACPI driver for "hot add" memory event. The ACPI driver responds to the "hot add" memory event by performing the 5 tasks, wherein the first task is to determine if memory has been added or removed and if the has been added, determine whether if it is a "hot addition" or a "hot replacement". This task is equivalent to what is claimed by identifying a memory module, which is being added or removed from the computer system 10. Furthermore, tasks 2-5 performing the memory configuration for the "hot add" memory event).

Adding the identified caching agents of the hot plug module to a resource pool of the running computing device (Column 5, lines 17-21, and column 3 lines 15-20, wherein the memory modules are added to the computer system as claimed).

Enabling communication interface on the hot plug module to establish a communication link with the running computing device (Column 6, lines 50-57, and

column 5 lines 1-23, wherein the 5 tasks performing the configuration for establishing communication between the newly added memory module and the computer system 10).

Claims 1-5, 7-10, 28-29, 35, and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Bealkowski et al. ("Bealkowski") (U.S. Patent No. 6,282,596).

As for claims 1 and 8, Bealkowski teaches a method of adding one or more caching agents to a running computing device (see figure 1-3, hot plug processor cards 11, 20, 30 and column 3 lines 9-11, column 4 lines 4-11, wherein each processor card is hot plug and each processor card comprises a cache), comprising identifying the one or more caching agents provided by a hot plug module in response to the hot plug module being physically coupled to the running computing device (see figure 4 and column 7 line 51 to column 8 line 31, wherein each processor is identified with an agent ID and the hot plug controller uses the agent ID identify which processor card is removed or inserted to the computer system); and adding the identified caching agents of the hot plug module to a resource pool of the running computing device (see figure 2, service processor 31 and column 5 lines 31-60, wherein the service processor 31 controls the hot plug controller and also monitoring the events in the computer such as insertion or removal and then stores such information to its own associated memory and controller routine. Further, column 3 lines 35-41, teaches integrated processor cards which including cache into the data processing. Therefore, the caches of the processor cards are considered adding memory to the data processing as well); and enabling a

communication interface on the hot plug module to establish a communication link with the running computing device (see figures 1-3, processor cards 11, 20, 30 are hot plugged to the data processing system 10 via the CPU connectors. Further, data processing system 10 supports hot plugging and initializing processor cards for communication between the newly added processor card and the processing system 10 via the CPU connectors as discloses in column 3 lines 1-15 and lines 32-41, and Column 6 lines 35-39).

As for claims 2 and 9, Bealkowski further teaches comprising enabling a communication interface (Figure 3, item 14a-d) of the running computing device (Column 3, lines 27-29) that is associated with the hot plug module in response to determining that the hot plug module has been physically coupled to the running computing device (see figure 4, wherein the flow chart describes the processor for establishing communication between the processor cards and the computer system; Column 7 line 51 – Column 8 line 30).

As for claims 3 and 10, Bealkowski teaches performing a self test of the hot plug module, and in response to passing the self test, enabling the communication interface of the hot plug module to establish a communication link with the communication interface of the running computing device (see column 8 lines 31-39).

As for claim 4, Bealkowski teaches initializing the hot plug module, and after initializing the hot plug module, enabling the communication interface of the hot plug module to establish a communication link with the communication interface of the running computing device (see column 9 lines 10 lines 4-10).

As for claim 5, Bealkowski teaches wherein adding comprises adding one or more memory caching processors of the identified caching agents to a processor pool of the running system (see column 5 lines 53-60 and Column 4, lines 3-6).

As for claim 7, Bealkowski teaches identifying memory of the hot plug module in response to the hot plug module being physically coupled to the running computing device; and adding the identified memory of the hot plug module to a memory pool of the running computing device to increase the memory pool from which memory is allocated to processes (see Column 9, lines 42-45 and Column 3, lines 35-41).

As for claim 28, Bealkowski teaches a computing device comprising, a midplane comprising a coupler and a hot plug interface to track a state associated with the coupler (see figure 1); a hot plug module comprising a coupler to detachably couple the hot plug module to the coupler of the midplane and resources coupled to the coupler of the hot plug module via a hot plug interface of the hot plug module (see figure 1, processor cards are connected to the CPU connectors 14 to the system bus 18), the hot plug module to update the state of the hot plug interface of the midplane to indicate

when the resources are ready to join the computing device (see column 5 lines 41-52); and a processor coupled to the hot plug interface of the midplane (see figure 1, service processor 31), the processor to add the resources to the computing device without rebooting in response to determining that the hot plug interface of the midplane indicates the resources are ready to join (see column 1 lines 57-58, Column 3 lines 32-41, and Column 6, lines 31-39).

As for claim 29, Bealkowski teaches wherein the midplane comprises a hot plug monitor that provides the hot plug interface of the midplane with a signal indicative of whether the coupler of the hot plug module has been coupled to the coupler of the midplane, and the processor programs the hot plug interface of the midplane to generate a hot plug interrupt in response to a change in the signal that is indicative of whether the coupler of the hot plug module has been coupled to the coupler of the midplane (see column 8 lines 1-5; ie. CFG signal).

As for claims 35 and 37, Bealkowski teaches transferring packets between the communication interface on the hot plug module and the communication interface of the running computer system to establish the communication link (Column 4 lines 38-46; ie. since the bus [by which the processor cards 11a-d communicate with the running computer system, see Figure 2] operates according to the PCI specification, the data traveling to and from processor cards 11a-d must inherently be in the form of packets, as evidenced by the PCI Local Bus Specification, Revision 2.2, December 18, 1998,

see for example Page 26 [FRAME#] and also Pages 30-31 [Configuration Commands of Type 0 and Type 1], cited below under Relevant Art).

Relevant Art

PCI Local Bus Specification, Revision 2.2, December 18, 1998, pages 26-32 is cited as Relevant Art.

(10) Response to Argument

Appellant's arguments filed 10/6/2006 regarding the rejection to Claims 1 and 7-9 as being anticipated by Olarig have been fully considered but they are not persuasive. Appellant argues that "a person skilled in the art would not interpret 'circuitry on the memory module is fully turned on before the circuitry is driven by a clock signal' as being similar to 'enabling a communication interface on a hot plug module to establish a communication link with a running computing device'." The examiner disagrees. Contrary to Appellant's argument, in the cited section (Column 6, lines 50-57) the newly added memory module is not enabled to communicate with the computer system (ie. transfer data to/from other components in the system) until the circuitry on the memory module is fully turned on. Further, the term "enabling" is a broad term, which can be taken to mean simply to allow a function to be performed. In the context of the Olarig reference, the "enabling" function can be equated to the computer system 10 sending a signal to activate power within memory modules 14 as they are inserted into slots 16. Therefore, Appellant's argument regarding this limitation is not persuasive.

Appellant's arguments filed 10/6/2006 regarding the rejection to Claims 1-5, 7, 8, 28-29, and 35-37 as being anticipated by Bealkowski have been fully considered but they are not persuasive.

Regarding Claims 1, 5, and 8, Appellant argues that "the processor cards 11a-11d appear not to have a communication interface." The examiner disagrees. Contrary to Appellant's argument, the processor cards 11a-11d communicate on the bus 18 and therefore must necessarily have input/output capabilities in order for that communication to occur (ie. that each of the processor cards 11a-11d must have a communication interface to connect to CPU connectors 14a-d). Appellant also argues that "Bealkowski does not explicitly or inherently teach that such an interface is enabled in order to establish a communication link." The examiner disagrees. Contrary to Appellant's argument, Bealkowski teaches supplying power along with a clock signal to processor cards 11a-11d once a processor card is coupled to the system bus 18, see Column 3 lines 32-41 and Column 6 lines 35-39, which is equivalent to enabling the communication interface on the processor card. Further, as discussed with regards to the Olarig reference above, "enabling" can be taken to mean simply to allow a function to be performed. In the context of the Bealkowski reference, the "enabling" function can be equated to the computer system (Figure 1/Figure 2 item 10) sending a signal to activate power within processor cards 11a-d as they are inserted into CPU connectors 14a-d. Therefore, Appellant's argument regarding these limitations is not persuasive.

Regarding Claims 2-4, Appellant argues that "[t]he examiner appears to equate CPU connector 14 of Bealkowski with communication interface of a hot plug module of the Appellants." Contrary to Appellant's argument, as described above, the processor cards 11a-d must necessarily have there own communication interfaces in order to transfer data to/from CPU connectors 14a-d. Further, the claim language states "enabling a communication interface *of the running computing device* that is associated with the hot plug module", which Bealkowski also discloses in enabling a communication interface (Figure 3, item 14a-d) of the running computing device (Column 3, lines 27-29) that is associated with the hot plug module in response to determining that the hot plug module has been physically coupled to the running computing device (Figure 4, Column 7 line 51 – Column 8 line 30). Therefore, Appellant's argument regarding this limitation is not persuasive.

Regarding Claim 7, Appellant argues that "Bealkowski, in column 9, lines 42-45, only teaches that in removing the processor from operation, the work load is quiesced from the processor, the caches of the processor are flushed and the processor is set to idle" and that "Bealkowski does not appear to teach, 'identifying memory of the hot plug ... memory is allocated to process." The examiner disagrees. Contrary to Appellant's argument, Bealkowski teaches adding memory from a hot plug module to a memory pool of the running computing device to increase the memory pool from which memory is allocated to processes in Column 9, lines 42-45. Bealkowski teaches that the processor caches are flushed to remove the work load from the processor of the hot plug module. Therefore, this citation alone indicates that since the caches of the

processor cards 11a-d need to be flushed when the card(s) are removed, that they were in fact being used in the memory pool before it was taken out of the system. In addition, Column 3, lines 35-41 (ie. "additional processor subsystems are integrated into the data processing system...") also teaches this limitation. Therefore, Appellant's argument regarding this limitation is not persuasive.

Regarding Claim 28, Appellant argues that "Bealkowski does not appear to teach, 'the processor to add the resource to the computing device ... resources are ready to join'". The examiner disagrees. Contrary to Appellant's argument, since Bealkowski teaches enabling a communication interface on the hot plug module to establish a communication link with the running computing device, as described above in the discussion of Claim 1, Bealkowski similarly teaches the limitation "the hot plug module to update the state of the hot plug interface of the midplane to indicate when the resources are ready to join the computing device". Further, by selectively enabling the processor cards 11a-d, the system must have knowledge of when the resources (ie. the caches of the processor cards 11a-d) are ready to join, see Column 3 lines 32-41 and Column 6, lines 31-39. Still further, Bealkowski teaches LEDs that indicate if the processor cards 11a-d are functioning properly (e.g. if the LED is green, that processor card is ready to join), see Column 5, lines 41-52. Therefore, Appellant's argument regarding this limitation is not persuasive.

Regarding Claim 29, Appellant argues that Bealkowski does not teach a "hot plug interface of the midplane to generate a hot plug interrupt in response to a change in the signal that is indicative of whether the coupler of the hot plug module has been coupled

to the coupler of the midplane." The examiner disagrees. Contrary to Appellant's argument, Bealkowski does in fact teach this limitation, see Column 8, lines 1-5 (ie. the CFG signal is sent when a processor card 11a-d is added). Therefore, Appellant's argument regarding this limitation is not persuasive.

Regarding Claims 35 and 37, Appellant argues that Bealkowski does not teach "transferring packets between the communication interface on the hot plug module and the communication interface of the running computer system." The examiner disagrees. Contrary to Appellant's argument, since the bus (by which the processor cards 11a-d communicate with the running computer system, see Figure 2) operates according to the PCI specification, see Column 4 lines 38-46, the data traveling to and from processor cards 11a-d must inherently be in the form of packets, as evidenced by the PCI Local Bus Specification, Revision 2.2, December 18, 1998, see for example Page 26 (FRAME#) and also Pages 30-31 (Configuration Commands of Type 0 and Type 1). In the PCI Specification, a FRAME# is defined as a signal that "is driven by the master to indicate the beginning and end of a transaction." Thus, a transaction is only completed according to the boundaries defined by a "frame". Therefore, Appellant's argument regarding this limitation is not persuasive.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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